AF/ JRW

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/733,799
Filing Date	December 12, 2003
First Named Inventor	Takashi NOMA
Art Unit	2818
Examiner Name	D. Vu
Attorney Docket Number	606402015200

Total Number of Pages in This Submission

ENCLOSURES (*Check all that apply*)

- [x] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
- [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please identify below):

Appellant's Opening Brief
Return Receipt Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	MORRISON & FOERSTER LLP		
Signature	for Barry Reg. #45,640		
Printed name	Barry E. Bretschneider		
Date	May 4, 2006	Reg. No.	28,055

PTO/SB/17 (01-06)
Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
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METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 03-1952 Deposit Account Name: Morrison & Foerster LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

FEE CALCULATION (All the fees below are due upon filing or may be subject to a surcharge.)

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	**Fee ($)**	**Small Entity Fee ($)**
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
_____	- 20 =	_____	x _____	=	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
_____	- 3 =	_____	x _____	=	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims

Fee ($)	**Fee Paid ($)**
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**	**Fee ($)**	**Fee Paid ($)**
_____	- 100 =	_____	/50	_____ (round up to a whole number) x	_____	= _____

4. OTHER FEE(S) **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount)

Other (e.g., late filing surcharge): 1402 Filing a brief in support of an appeal 500.00

SUBMITTED BY					
Signature	Barry Bretschneider Reg. #45,640	Registration No. (Attorney/Agent)	28,055	Telephone	(703) 760-7743
Name (Print/Type)	Barry E. Bretschneider			Date	May 4, 2006

va-161879

PATENT
Docket No. 606402015200

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In the application of:

Takashi NOMA

Serial No.: 10/733,799

Filing Date: December 12, 2003

For: SEMICONDUCTOR DEVICE MANUFACTURING METHOD

Examiner: David Vu

Group Art Unit: 2818

Conf. No.: 8803

APPELLANT'S OPENING BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a timely appeal from the final rejection of claims 1, 3 and 4 in this application.

I. REAL PARTY IN INTEREST

The real party in interest is Sanyo Electric Co., Ltd., of Osaka, Japan, the assignee of appellant's entire, right, title and interest in this application.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences within the meaning of 37 CFR 41.37(c)(1)(ii) known to appellant or his undersigned counsel.

III. STATUS OF CLAIMS

Claims 1 and 3-10 are pending in this application. Claims 5-10 have been allowed.

Claims 1, 3 and 4 (reproduced in the attached Appendix) have been finally rejected under 35 USC 102(b).

IV. STATUS OF AMENDMENTS

Appellant filed an Amendment Under 37 CFR 1.111 on August 30, 2005, which was entered, and a Response Under 37 CFR 1.116 on February 2, 2006, so the claims on appeal stand as amended in the Amendment filed August 30, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This invention is a method of heating a semiconductor wafer in a reflow process so that reflow of metal portions placed on the semiconductor wafer is performed uniformly to form conductive terminals. A reflow process forms conductive terminals by heating metal deposits, such as those made by screen printing, formed on the surface of the semiconductor wafer relying on the surface tension of the molten metal deposits. When a semiconductor wafer is deformed during its manufacturing process, the formation of conductive terminals on such a deformed semiconductor wafer by a reflow process does not result in the consistent formation of the conductive terminals over the entire area of the semiconductor wafer. In the prior art reflow process such as the one shown in FIG. 13 of the application, the semiconductor wafer 124 is directly placed on stage 123 that is placed in reflow furnace 120. Appellant found that thermal conduction paths are different between the deformed portion of the semiconductor wafer 126 that is not in contact with the stage 123 and the non-deformed portion of the semiconductor wafer 125 that is in contact with the stage 123, as shown in FIG. 14 of the application. This results in non-uniform heating of the semiconductor wafer 124 and the metal deposits formed on the surface of the semiconductor wafer 124, which gives rise to inconsistent conductive terminal formation.

The invention is directed to improving the uniformity of the reflow heating of a deformed semiconductor wafer by placing the semiconductor wafer 1a on pins 21 that stand on stage 20 of reflow furnace 30, as shown in FIGS. 6A and 6B of the application. In the embodiment

explained in the specification, metal deposits 9 are screen printed on the surface of the semiconductor wafer 1a as shown in FIG. 5. The semiconductor wafer 1a is placed on the pins 21 standing on the stage 20. The wafer-stage assembly is placed on belt 31 of the reflow furnace 30 and is led to heating zone 41 of the reflow furnace 30 by the belt 31. When it passes through the heating zone 41, the semiconductor wafer 1a is heated by IR heaters 45, hot plates 46 and side heaters 47 that are placed respectively on the ceiling, the floor and the sidewall of the reflow furnace 30. This heating is more uniform than the heating of the prior art reflow furnace because the semiconductor wafer 1a is elevated from the stage 21 and thus receives similar thermal radiations from all directions, as shown in FIG. 8 of the application.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether the Examiner erred in rejecting claims 1, 3 and 4 under 35 USC 102(b) on Chroneos.

VII. ARGUMENT

A. Claims 1, 3 and 4 Are Not Anticipated by Chroneos Because Chroneos Does Not Disclose Claimed Semiconductor Wafer.

To anticipate a claim, the reference must teach every element of the claim. MPEP 2131. Accordingly, the standard for the anticipation analysis is that "[e]very element of the claimed invention must be literally present, arranged as in the claim. ... The identical invention must be shown in as complete detail as is contained in the patent claim." *Richardson v. Suzuki Motor Co., Ltd.*, 868 F.2d 1226, 1236 (Fed. Cir. 1983).

Claim 1 recites suspending the semiconductor wafer on a plurality of pins in a reflow furnace so that the metal portions are positioned upwardly in the reflow furnace. The Examiner relies on Chroneos for the teachings of the claimed reflow method, including the suspension on pins of the semiconductor wafer of claim 1.

Chroneos teaches a surface mountable pin connector 100 that includes carrier 102, which carries a substrate, a circuit board or the like, and metal pins 116 which are soldered into the carrier 102 and provide electrical connection for the device the carrier 102 carries. A surface

mount assembly 202 is mounted on this pin connector 100 via solder balls 120 so that the surface mount assembly 202 can have electrical connections with external devices through the metal pins 116, as shown in FIG. 2. Prior to the mounting of the surface mount assembly 202 to the pin connector 100, the solder balls 120 are reflowed so as to adhere to metallized lands 114 formed on the carrier 102. Chroneos explains at column 2, lines 53-56, that the carrier 102 is made of a FR4 laminate material that is used for making a printed circuit board (PCB).

The Examiner equated the claimed semiconductor wafer to Chroneos' carrier 102. This element of claim 1, the semiconductor wafer, is not "literally present" in Chroneos because a carrier that is made of a FR4 laminate material is not a "semiconductor wafer." Chroneos' method is not "identical" in this aspect of the claimed invention. Accordingly, the claimed invention is not anticipated by Chroneos because Chroneos does not teach at least one of the elements of the claimed invention, *i.e.*, suspending the semiconductor wafer on a plurality of pins in a reflow furnace so that the metal portions on the semiconductor wafer are positioned upwardly in the reflow furnace.

B. The Examiner's Contention That A Printed Circuit Board Corresponds To A Semiconductor Wafer Is Not Reasonable.

During the examination of a patent application, "claims must be given their broadest reasonable interpretation." MPEP 2111. However, "[a]lthough the PTO must give claims their broadest reasonable interpretation, this interpretation must be consistent with the one that those skilled in the art would reach." *In re Cortright*, 165 F.3d 1353, 1358 (Fed. Cir. 1999).

In the Advisory Action mailed February 16, 2006, the Examiner contended, in response to appellant's argument in section VII.A. above, that the claimed semiconductor wafer corresponds to Chroneos' carrier 102 made of a FR4 laminate material because "the silicon/semiconductor wafer is well known material for forming the substrate/PCB layer in a method of manufacturing a semiconductor device (See Chroneos, Jr.; US 6,259,039; col. 2, lines 59-61)." The Examiner's argument is not reasonable.

First, no person of ordinary skill in the art would have understood that a semiconductor wafer is a material for forming the PCB layer. A semiconductor wafer is made of a semiconductor material such as silicon, while the material of a PCB, including a FR4 laminate, is made of an organic material such as an epoxy resin. They are different materials. A PCB cannot be and is not made out of a silicon wafer, contrary to the Examiner's argument. Second, the cited portion of Chroneos states that "[s]uch alternative PCB materials and metallization material are well known in the art and will not be described further herein." This statement in no way teaches persons of ordinary skill in the art that a semiconductor wafer may be used as a material for making a PCB. The Examiner does not explain how this statement provides such a teaching to persons of ordinary skill in the art.

The Examiner's contention that a printed circuit board corresponds to the claimed semiconductor wafer is not reasonable because his broad reading of the term "a semiconductor wafer" is not "consistent with the one that those skilled in the art would reach."

C. The Specification Does Not Change The Plain Meaning of "Semiconductor Wafer".

The words of a claim must be given their plain meaning unless they are defined in the specification. MPEP 2111.01. The MPEP further explains that "the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention," citing *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). The ordinary and customary meaning of "semiconductor wafer" to persons of ordinary skill in the art does not include a printed circuit board, as explained in VII.C. The specification does not change the ordinary and customary meaning of the term "semiconductor wafer" in any way. The Examiner did not point to any portion of the specification to show that appellant has changed the ordinary and customary meaning of a semiconductor wafer. Thus, the meaning of the term "semiconductor wafer" does not include a printed circuit board.

The Examiner erred in rejecting claims 1, 3 and 4 under 35 USC 102(b) on Chroneos because Chroneos does not teach or suggest the claimed suspension of the semiconductor wafer on a plurality of pins in a reflow furnace.

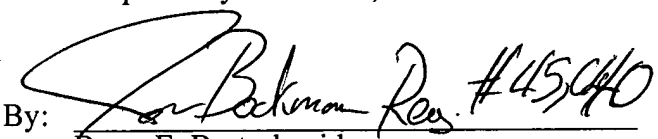
CONCLUSION

For the foregoing reasons, the Board should reverse the final rejection of claims 1, 3 and 4 in this application.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, appellant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. **606402015200**.

Respectfully submitted,

Dated: May 4, 2006

By: 

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APPENDIX OF CLAIMS ON APPEAL

1. A semiconductor device manufacturing method, comprising:

providing a semiconductor wafer provided with a plurality of metal portions on a surface of the semiconductor wafer;

suspending the semiconductor wafer on a plurality of pins in a reflow furnace so that the metal portions are positioned upwardly in the reflow furnace;

reflowing the metal portions on the surface of the semiconductor wafer suspended in the reflow furnace so that the metal portions form conductive terminals using a first heater disposed in the reflow furnace and facing the surface of the semiconductor wafer.

3. The semiconductor device manufacturing method of claim 1, wherein the pins are mounted on a stage that is heated by a heating plate disposed under the stage.

4. The semiconductor device manufacturing method of claim 1, wherein the semiconductor wafer is heated by a second heater disposed so as to face a lateral edge of the semiconductor wafer.

EVIDENCE APPENDIX

[NONE.]

RELATED PROCEEDINGS APPENDIX

[NONE.]